WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of memory cell array regions arranged in matrix, spaced apart from each other in a row direction and in a column direction, on a semiconductor substrate;

a plurality of sense amplifier regions each arranged in a gap between said memory array regions in said column direction and provided with a sense amplifier-forming element;

a plurality of subdecoder regions each arranged in a gap between said memory cell array regions in said row direction;

a plurality of intersection regions each positioned at an intersection of said plurality of sense amplifier regions in line and said plurality of subdecoder regions in line; and

a plurality of sense amplifier driver elements each arranged in said subdecoder region for use in an operation of said sense amplifier.

2. The semiconductor memory device according to claim 1 wherein in an end portion in said column direction of a region provided with said plurality of memory cell array regions, said sense amplifier driver elements are dispersedly arranged in said subdecoder region adjacent to said end portion and a region on the outer side of said region provided with said plurality of memory cell array regions.

3. The semiconductor memory device according to claim 1 wherein said sense amplifier driver elements are dispersedly arranged in said subdecoder region and said intersection region.

4. The semiconductor memory device according to claim 1 further comprising:

a conductive impurity diffusion region formed in said semiconductor substrate and including a portion exposed on a main surface of said semiconductor substrate in said subdecoder region; and

a potential fixing conductor connected to said portion exposed in said subdecoder region for determining a potential of said conductive impurity diffusion region.

5. The semiconductor memory device according to claim 1 wherein said sense amplifier driver elements for use in an operation of a sense amplifier formed in one of a plurality of said sense amplifier regions are dispersedly arranged in two of said subdecoder regions positioned such that said intersection region adjacent to said one of said sense amplifier regions is interposed therebetween.

6. The semiconductor memory device according to claim 1 wherein

in said sense amplifier region, a main surface of said semiconductor substrate includes a first conductivity type region and a second conductivity type region that are adjacent to each other,

in said sense amplifier region, a plurality of said sense amplifier-forming elements are arranged in one of said first conductivity type region and said second conductivity type region, and

for a plurality of particular elements formed in one of said first conductivity type region and said second conductivity type region, of said plurality of sense amplifier-forming elements, respective distances from a boundary portion between said first conductivity type region and said second conductivity type region to said particular elements are substantially equal.